ALUPE UNIVERSITY COLLEGE

...Bastion of Knowledge...

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OFFICE OF THE DEPUTY PRINCIPAL
ACADEMICS, STUDENT AFFAIRS AND RESEARCH

UNIVERSITY EXAMINATIONS

2018 /2019 ACADEMIC YEAR

FIRST YEAR SECOND SEMESTER REGULAR EXAMINATION

FOR THE DEGREE OF BACHELOR OF COMPUTER SCIENCE

COURSE CODE: **COM 120**

COURSE TITLE: **System software**

DATE: 16th April, 2019   **TIME: 9:00AM-12:00pm**

INSTRUCTION TO CANDIDATES

- **SEE INSIDE**

THIS PAPER CONSISTS OF 4 PRINTED PAGES   **PLEASE TURN OVER**

A constituent college of Moi University

COM 120: SYSTEM HARDWARE

<u>STREAM: BSc (Computer Science)</u>   <u>DURATION: 3 Hours</u>

<u>INSTRUCTIONS TO CANDIDATES</u>

  i.   *Answer **ALL** questions from section A and any **THREE** from section B.*

  ii.   *Maps and diagrams should be used whenever they serve to illustrate the answer.*

  iii.   *Do not write on the question paper.*

<u>SECTION A (24 MARKS) COMPULSORY</u>

QUESTION ONE (12 Marks)

a) (i) List 6 applications that lead to the need for personal computers as we know them today to be designed with enhanced power (3 Marks)

     (ii) With regards to computer chip organization and microcomputer architectural design for performance, distinguish between the pipelining design approach and superscalar design approach. (4 Marks)

b) With the aid of well labelled diagrams, show the difference between programming in hardware and programming in software during the design and development of computer systems. (2 Marks)

c) With regards to machine instruction set, state one advantage and one disadvantage associated with the machine instruction set. (3 Marks)

QUESTION TWO (12 Marks)

a) Describe the two main causes for performance degradation on a computer system whose motherboard has been attached to a great number of devices. (4 Marks)

b) Many processor designs include a register or set of registers, often known as the program status word (PSW), that contain status information. State three Common fields or flags associated with the PSW. (3 Mark)

c) The two stage instruction pipelining employs the instruction prefetch or fetch overlap approach with the aim of doubling execution time. Give three reasons why the aforementioned doubling of execution time is usually not attained. (3 marks)

d) State the two basic tasks performed by a microprogrammed control unit (2 Marks)

SECTION B (36 Marks)

QUESTION THREE (12 Marks)

a) In 1946, von Neumann and his team of scientists began the design of a revolutionary new stored-program computer, referred to as the IAS computer, at the Princeton Institute for Advanced Studies. The IAS computer, although not completed until 1952, became the prototype of all subsequent general-purpose computers. With the aid of a well labelled diagram describe the general structure of the IAS computer. (4 Marks)

b) Describe the four registers that are involved when an instruction is fetched from memory.

(4 Marks)

c) Outline the four categories in which a micro-operations may fall under (4 Marks)

QUESTION FOUR (12 Marks)

a) Consider a scenario where the program reaches a point at which it makes a system call in the form of a WRITE call. After these few instructions have been executed, control returns to the user program. Meanwhile, the external device is busy accepting data from computer memory and printing it. This I/O operation is conducted concurrently with the execution of instructions in the user program. When the external device becomes ready to accept more data from the processor,—the I/O module for that external device sends an interrupt request signal to the processor. Provide a brief explanation of how the processor would handle such an interrupt (4 Marks)

b) Describe the five activities that a processor needs to conduct while fulfilling its required duties. (5 Mark)

c) Outline the three-step process that leads to a characterization of the control unit

(3 Marks)

QUESTION FIVE (12 Marks)

a) (i) Describe how a horizontal microinstruction can be achieved as part of firmware

(4 Marks)

(ii) Provide a detailed discussion of the principal advantage associated with microprogramming (4 Marks)

b) Describe four Registers that play an essential role in instruction Execution (4 Marks)

QUESTION SIX (12 Marks)

a) A pipeline bubble occurs when the pipeline, or some portion of the pipeline, must stall because conditions do not permit continued execution. Discuss the three types of hazards associated with a pipeline bubble (6 Marks)

b) When Indexing is adopted as a form of displacement addressing within the memory it provides an efficient mechanism for performing iterative operations. Now consider a scenario where a list of numbers are stored starting at location A. Suppose that we would like to add 1 to each element on the list. Explain how displacement addressing employing the Indexing method would handle such an operation (6 Marks)

QUESTION SEVEN (12 Marks)

a) With the aid of a well labelled diagram, provide a detailed description of High Performance Mezzanine architecture (12 Mark)

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