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OFFICE OF THE DEPUTY PRINCIPAL
ACADEMICS, STUDENT AFFAIRS AND RESEARCH

UNIVERSITY EXAMINATIONS
2017 /2018 ACADEMIC YEAR

FIRST YEAR SECOND SEMESTER REGULAR EXAMINATION

FOR THE DEGREE OF BACHELOR OF SCIENCE IN COMPUTER SCIENCE

COURSE CODE: **COM 120**
COURSE TITLE: SYSTEM HARDWARE

DATE: 19TH APRIL, 2018 **TIME: 9AM – 12.00 NOON**

INSTRUCTION TO CANDIDATES

- **SEE INSIDE**

THIS PAPER CONSISTS OF 3 PRINTED PAGES **PLEASE TURN OVER**

COM 120: SYSTEM HARDWARE

STREAM: COMPUTER SCIENCE **DURATION: 3 Hours**

INSTRUCTIONS TO CANDIDATES

i. *Answer Question **ONE** and any other **TWO** questions.*

ii. *Maps and diagrams should be used whenever they serve to illustrate the answer.*

iii. *Do not write on the question paper.*

SECTION A (24 MARKS) COMPULSORY

QUESTION ONE (12 Marks)

(a) Describe the role of each of the following pieces of hardware within the computer system
(i) MBR (ii)MAR (iii) IR

(iv) IBR (v) PC (Vi) AC (12 marks)

QUESTION TWO (12 Marks)

(a) A user-visible register is one that may be referenced by means of the machine language that the processor executes. Describe the four categories in which a user-visible register can be characterized. (8 marks)

(b) Identify the four control signals that are sent simultaneously by the control unit when it is reading a word from memory into the MBR (4 Marks)

SECTION B (36 MARKS) ATTEMPT ANY THREE QUESTIONS

QUESTION THREE (12 Marks)

(a) When Indexing is adopted as a form of displacement addressing within the memory it provides an efficient mechanism for performing iterative operations. Now consider a scenario where a list of numbers are stored starting at location A. Suppose that we would like to add 1 to each element on the list. Explain how displacement addressing employing the Indexing method would handle such an operation (6 Marks)

(b) Instruction pipelining may speed up instruction execution only if the fetch and execute stages are of equal duration, the instruction cycle time would be halved. However, this doubling of execution rate is unlikely for 3 reasons. Identify the aforementioned three reasons (6 marks)

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QUESTION FOUR (12 Marks)

(a) The fetch instruction is usually loaded into the IR register wich interprets the instruction and performs the required action. Outline the four cartegories in which this action may fall into (4 marks)

(b) With regards to the operations of a bus
(i) Identify two things a module must do if it wishes to send data to another (2 Marks)
(ii) Identify two things a module must do if it wishes to request for data from another module (2 Marks)

(c) Distinguish between hardwired implementation and microprogrammed implementation (4 Marks)

QUESTION FIVE (12 Marks)

(a) State the roles of the **clock**, **instruction register** and **flags** within the control unit (6 marks)

(b) Describe three separate parts of the computer system that act as a destination for signals (6 marks)

QUESTION SIX (12 Marks)

(a) Most systems need to be able to reference a large range of locations in main memory. For this, a variety of addressing techniques has to be employed. Identify the eight (8) most common addressing techniques as discussed in class (4 Marks)

(b) List the five (5) basic functional elements of the processor (5 marks)

(c) Identify the two (2) basic tasks performed by the control unit (3 Marks)

QUESTION SEVEN (12 MARKS)

(a) Pipelining performance cycle time can be determined as

$$t = \max [ti] + d = tm + d \quad 1 \ldots i \ldots k$$

Provide the representation of:
(i) ti =
(ii) tm =
(iii)k =
(iv)d = (8 Marks)

(b) Provide a brief sequential description of how the control unit performs its functions (4 Marks)

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